

METHOD FOR FORMING ENCAPSULATED METAL INTERCONNECT
STRUCTURES IN SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES

ABSTRACT OF THE DISCLOSURE

5 An advanced back-end-of-line (BEOL) integration scheme for semiconductor
devices using very low-k dielectric materials is disclosed. The disclosed method for
forming a metal interconnect structure in a semiconductor integrated circuit device
comprises forming the metal interconnects using a through-mask plating (TMP)
process, and encapsulating the interconnects with a barrier layer by selectively
10 depositing a barrier layer material using an electroless liner plating process or by
non-selectively depositing a blanket insulator diffusion barrier layer using PVD or
CVD techniques.